VISIT…

# STA543SA

## 24W x 1 + 7W x 2 Triple Amplifier with DC Volume Control

**PRELIMINARY DATA**

## Features

- OUTPUT POWER CAPABILITY
  24W x 1 + 7W x 2 @ $V_{CC}$ = 15V, $R_L$ = 4Ω, THD = 10%
- LINEAR DC VOLUME CONTROL FOR EACH SINGLE CHANNEL
- MINIMUM EXTERNAL COMPONENTS COUNT:
  - NO BOOTSTRAP CAPACITORS
  - NO BOUCHEROT CELLS
  - INTERNALLY FIXED GAIN (20dB SE, 26dB BTL)
- ST-BY FUNCTION (CMOS COMPATIBLE)
- NO AUDIBLE POP DURING ST-BY OPERATIONS
- DIAGNOSTIC FACILITIES
  - CLIP DETECTOR
  - OUT TO GND SHORT
  - OUT TO VS SHORT
  - SOFT SHORT AT TURN-ON
  - THERMAL SHUTDOWN PROXIMITY

### Protections

- OUPUT AC/DC SHORT CIRCUIT
- SOFT SHORT AT TURN-ON

**Clipwatt 19**

- OVERRATING CHIP TEMPERATURE WITH SOFT THERMAL LIMITER
- VERY INDUCTIVE LOADS
- FORTUITOUS OPEN GND
- ESD

## Description

The device is a class AB Audio amplifier assembled in the Clipwatt19 package; it is designed for high quality sound application.

The STA543SA is a 3-channels audio amplifier with DC volume control dedicated for each single channel. It is a device suitable for 2.1 solution thank to its output configuration with two single ended channels and one bridge. The Short Circuit Protection, the Thermal Protection and the Diagnostics Functions are integrated in the device.

## Order codes

| Part number | Temp range, °C | Package | Packing |
|---|---|---|---|
| STA543SA | 0 to 70 | Clipwatt 19 | Tube |



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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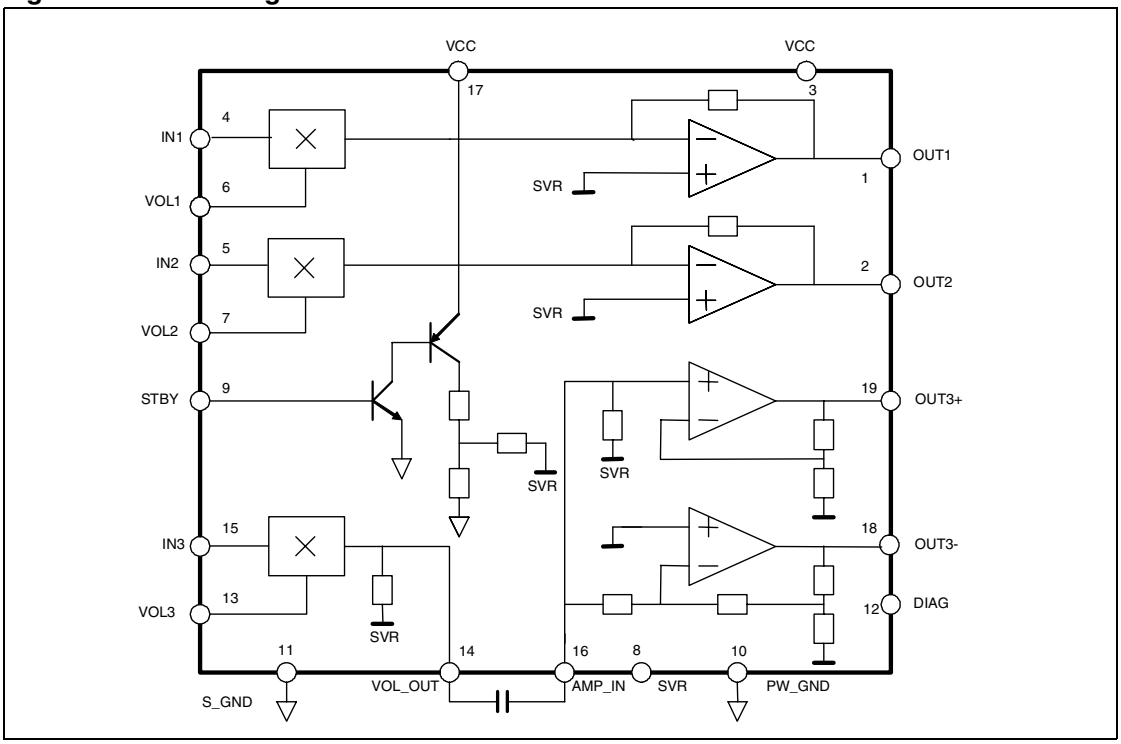
# 1 Block diagram and Pins description

## 1.1 Block diagram

**Figure 1. Block diagram**




## 1.2 Pins description

**Figure 2. Pins Connections** (Top view)

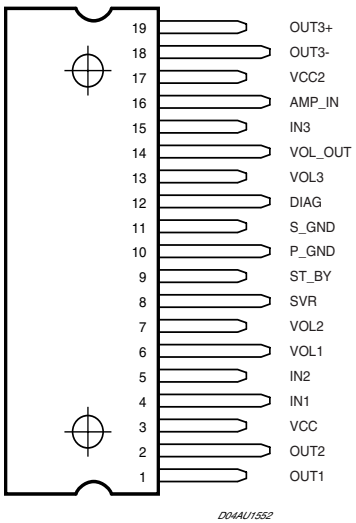


**Table 1. Pin description**

| N° | Pin Name | Pin Type | Function |
|---|---|---|---|
| 1 | OUT1 | OUTPUT | Channel 1 output |
| 2 | OUT2 | OUTPUT | Channel 2 output |
| 3 | VCC | POWER | Power supply |
| 4 | IN1 | INPUT | Channel 1 input |
| 5 | IN2 | INPUT | Channel 2 input |
| 6 | VOL1 | INPUT | Channel 1 volume control |
| 7 | VOL2 | INPUT | Channel 2 volume control |
| 8 | SVR | INPUT | Supply Voltage Rejection |
| 9 | ST-BY | INPUT | Stand-by |
| 10 | P_GND | POWER | Power ground |
| 11 | S_GND | POWER | Signal Ground |
| 12 | DIAG | OUTPUT | Diagnostics |
| 13 | VOL3 | INPUT | Channel 3 volume control |
| 14 | VOL_OUT | OUTPUT | Channel 3 volume control output |
| 15 | IN3 | INPUT | Channel 3 input |
| 16 | AMP_IN | INPUT | Channel 3 amplifier input |
| 17 | VCC2 | POWER | Power supply |
| 18 | OUT3- | OUTPUT | Channel 3 negative output |
| 19 | OUT3+ | OUTPUT | Channel 3 positive output |

# 2 Electrical specifications

## 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{op}$ | Operating Supply Voltage | 18 | V |
| $V_s$ | DC Supply Voltage | 20 | V |
| $P_{tot}$ | Total Power Dissipation ($T_{case}$ = 70°C) | 35 | W |
| $T_{stg}$, $T_j$ | Storage and Junction Temperature | -40 to150 | °C |
| $V_{ctr}$ | Volume Control DC Voltage | 7 | V |
| $T_{op}$ | Operating Temperature | 0 to 70 | °C |

## 2.2 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal Resistance Junction to case | Max. | 2 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal Resistance Junction to ambient | Max. | 45 | °C/W |

## 2.3 Electrical characteristics

**Table 4. Electrical characteristics**

(Refer to the test circuit, $V_S$ = 15V; $R_L$ = 4Ω; f = 1kHz; $T_{amb}$ = 25°C unless otherwise specified).

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply Voltage Range | | 8 | | 18 | V |
| $I_d$ | Total Quiescent Drain Current | | | | 150 | mA |
| $V_{os}$ | Output Offset Voltage | Single Ended<br>Bridge | -250<br>-150 | | 250<br>150 | mV |
| $P_o$ | Output Power | THD = 10%: $R_L$ = 4Ω<br>Bridge<br>Single Ended | | <br>24<br>7 | | <br>W<br>W |
| THD | Total Harmonic Distortion | $R_L$ = 4Ω, Single Ended,<br>Po =0.1 to 4W<br>Bridge, Po =0.1 to10W | | <br>0.4<br>0.4 | | <br>%<br>% |
| $C_T$ | Cross Talk | f = 1 kHz Single Ended<br>f = 10 kHz Single Ended | | 70<br>60 | | dB<br>dB |
| | | f = 1 kHz Bridge<br>f = 10 kHz Bridge | 55 | <br>60 | | dB<br>dB |
| $R_{in}$ | Input Impedance | Single Ended and Bridge | 20 | 30 | | kΩ |

**Table 4. Electrical characteristics** (continued)
(Refer to the test circuit, $V_S$ = 15V; $R_L$ = 4Ω; f = 1kHz; $T_{amb}$ = 25°C unless otherwise specified).

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $G_v$ | Maximum Voltage Gain Internally Fixed | Single Ended, Vol Ctrl (Pins 6 and 7) > 4.5V<br>Bridge, Vol Ctrl (pin 13) > 4.5V (**) | 19<br>25 | 20<br>26 | 21<br>27 | dB<br>dB |
| $A_{Min}$ Vol | Attenuation at minimum volume | Vol Ctrl < 0.5V | 80 | | | dB |
| $G_v$ | Voltage Gain Match | Single Ended | | | 0.5 | dB |
| $E_N$ | Total Output Noise | f = 20 to 22 kHz (play, max. volume)<br>Single Ended<br>Bridge | | 500<br>600 | | µV |
| | | f = 20 to 22 kHz (play, max. attenuation)<br>Single Ended<br>Bridge | | 250<br>500 | | µV |
| SVR | Supply Voltage Rejection | Rg = 0; f = 300Hz | 50 | | | dB |
| $A_{SB}$ | Stand-by Attenuation | | 80 | 90 | | dB |
| $I_{SB}$ | ST-BY Current Consumption | $V_{ST-BY}$ = 0 to 1.5V | | | 100 | µA |
| $V_{SB}$ | ST-BY In Threshold Voltage | | | | 1.5 | V |
| $V_{SB}$ | ST-BY Out Threshold Voltage | | 3.5 | | | V |
| $I_{stby}$ | ST-BY Pin Current | Play Mode $V_{stby}$ = 5V | | | 50 | µA |
| | | Max Driving Current Under Fault | | | 5 | mA |
| $I_{cd\ off}$ | Clipping Detector Output Average Current | d = 1% (*) | | 90 | | µA |
| $I_{cd\ on}$ | Clipping Detector Output Average Current | d = 5% (*) | | 160 | | µA |
| $V_{diag}$ | Voltage Saturation on DIAG | Sink Current at DIAG = 1mA | | | 0.7 | V |
| $T_W$ | Thermal Warning | | | 140 | | °C |
| $T_M$ | Thermal Muting | | | 150 | | °C |
| $T_S$ | Thermal Shut-down | | | 160 | | °C |

*Note: (*) DIAG Pulled-up to 5V with 10 kΩ; $R_L$ = 4Ω*

*(**) For channel 3: if used the input pin 16 (with 100nF decoupling) instead of pin 15 the voltage gain is always max. and it is independent from Volume Control.*

# 3 Test board and Layout

**Figure 3. Test board**

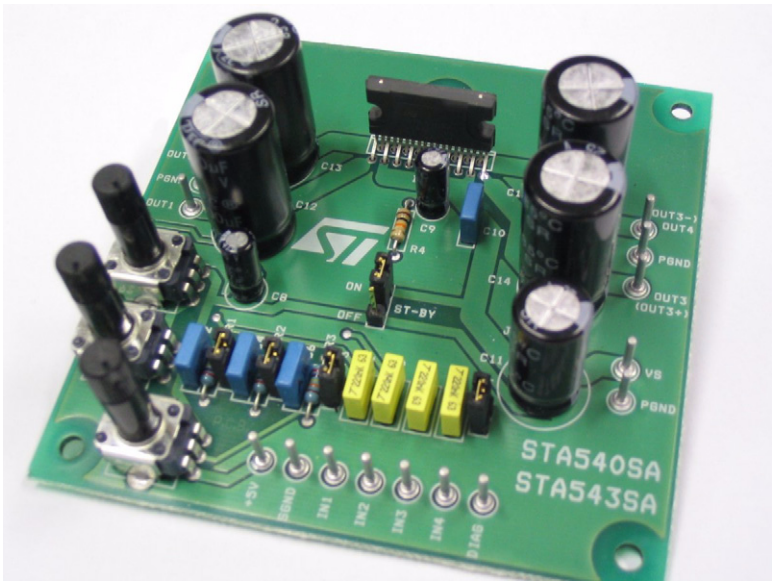
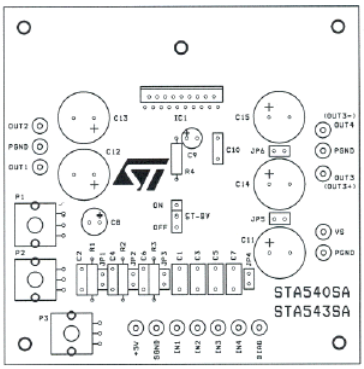
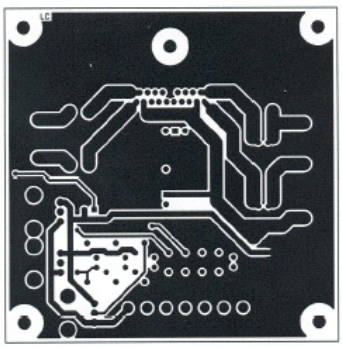


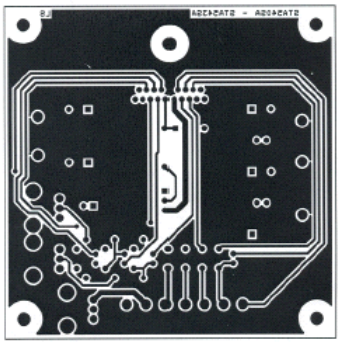

**Figure 4. PC boards and component layout**




Component layout

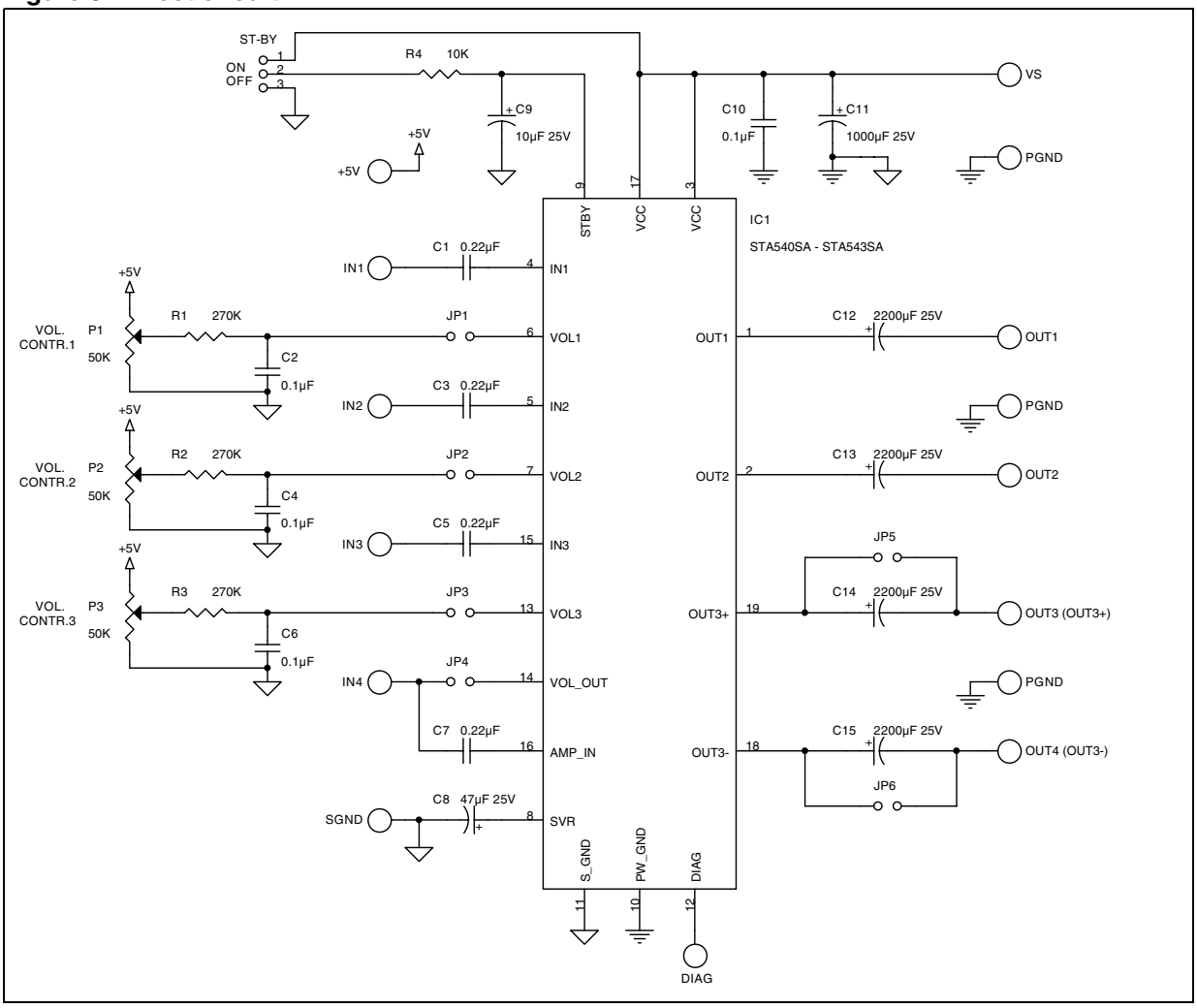


Component side



Solder side

**Figure 5. Test circuit**



## 3.1 Test board parts list

**Table 5. Test board parts list**

| Components | Suggested Value | Purpose |
|---|---|---|
| R1, R2, R3 | 300kΩ | DC Volume CTRL |
| R4 | 10kΩ | ST-BY TIME CONSTANT |
| P1, P2, P3 | 100kΩ | DC Vol. -CTRL |
| C2, C4, C6 | 0.1µF | Vol. -CTRL Bypass |
| C1,C3,C5,C7 | 0.22µF | INPUT DC DECOUPLING |
| C8 | 47µF | RIPPLE REJECTION |
| C9 | 10µF | ST-BY TIME CONSTANT |
| C10 | 0.1µF | SUPPLY VOLTAGE BYPASS |
| C11 | 1000µF | SUPPLY VOLTAGE BYPASS |
| C12,C13 | 2200µF | OUTPUT DC DECOUPLING |

**Table 6. Jumper selection**

| Jumpers | Purpose | Connection |
|---|---|---|
| JP1, JP2, JP3 | DC Volume CTRL | Closed |
| JP4 | Volume CTRL OUT | Closed |
| JP5, JP6 | Bypass DC out Capacitors | Closed connect BTL speaker Between Out 3+ And Out 3- |

# 4 Evaluation Board

In addition to the Test Board shown in *Figure 3.* intended also to evaluate the STA540SA Amplifier, it is possible to order the dedicated STA543SA evaluation board of *Figure 6.*

The PCB layout (single layer) is shown in *Figure 7.*

## 4.1 Crcuit description

With this board it is possible to amplify three analog signals Left, Right, Subwoofer coming from separated sources or to generate the BASS part to be sent to the Subwoofer via a passive crossover network.

All the three channels have a Linear DC volume Control.

**Figure 6. Evaluation Board Schematic**

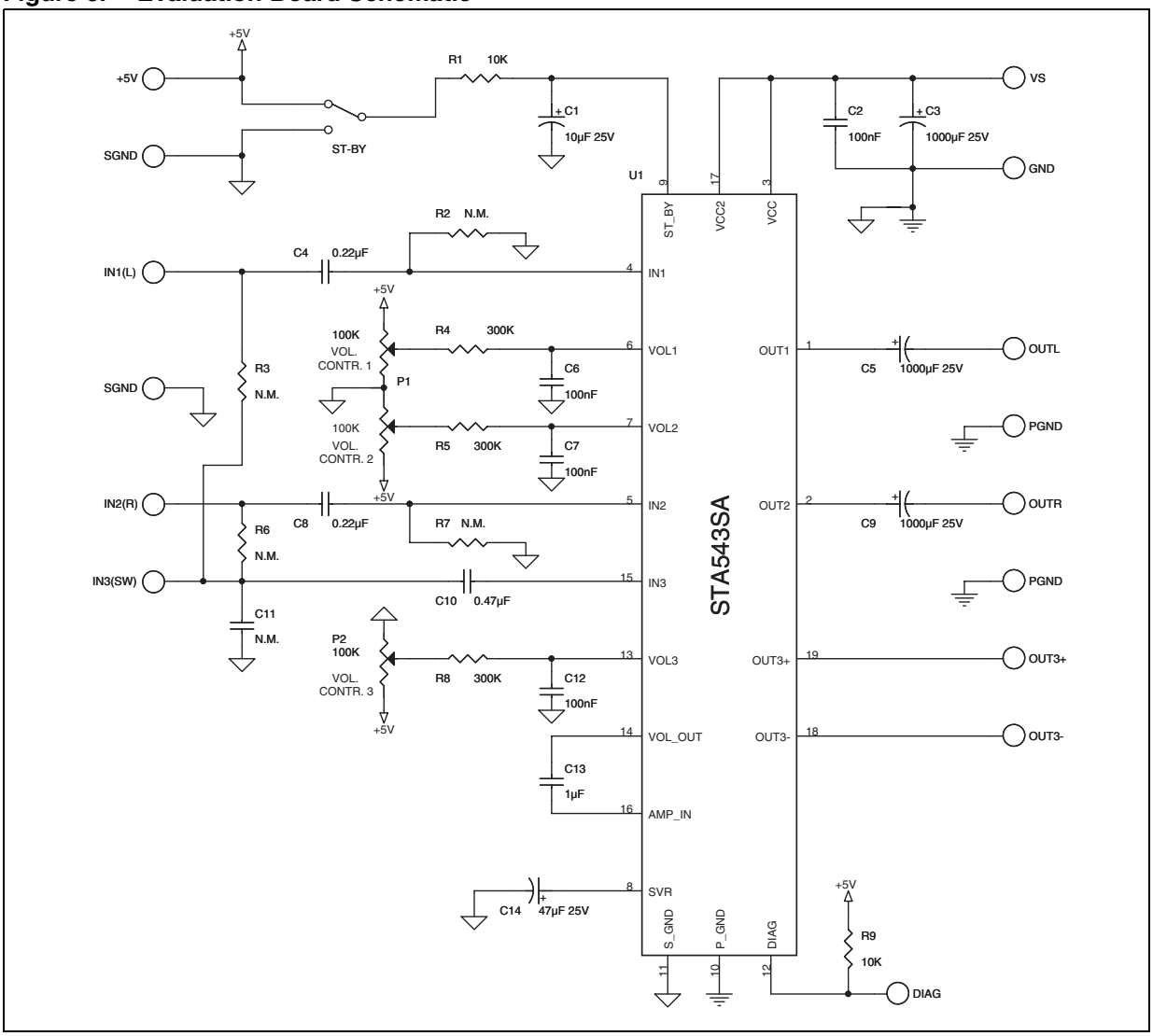
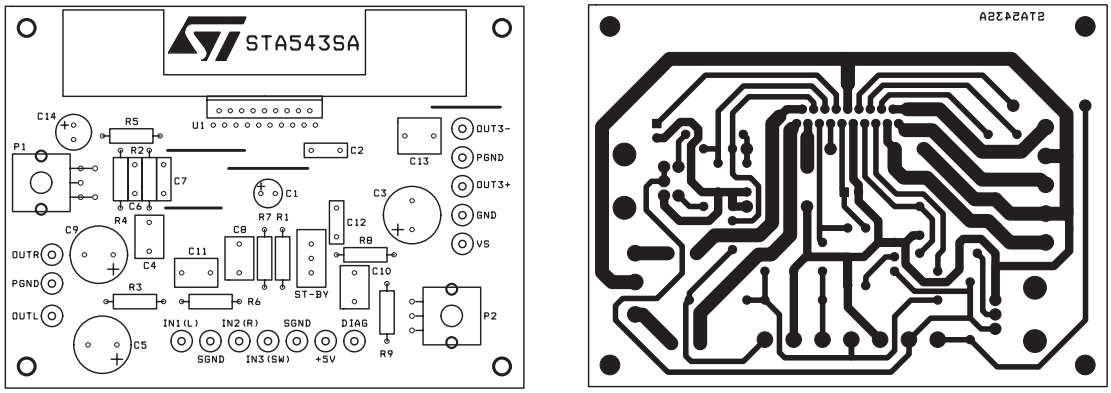


**Figure 7. Evaluation Board PCB and Component Layout**




Component Layout

PCB

**Table 7. Part list**

| Component | Recommended Value | Purpose | Larger than Recommended value | Smaller then Recommended value |
|---|---|---|---|---|
| R1 | 10K | St-By Circuit | Larger On/Off time | Smaller On/Off time |
| R2,R7 | Not mounted | See notes | | |
| R3,R6 | Not mounted | See notes | | |
| R4,R5,R8 | 300K | DC-Vol CTRL | | |
| P1,P2 | 100K pot. | DC-Vol CTRL | | |
| R10 | 10K | Open Collector Pull up | | |
| C1 | 10uF | St-by Circuit | Larger On/Off time | Smaller On/Off time |
| C2 | 100nF | Supply Voltage Bypass | | Danger of oscillations |
| C3 | 1000uF | Supply Voltage Bypass | | Danger of oscillations |
| C4,C8 | 220nF | Input DC decoupling L/R | Lower low freq Cutoff | Higher low freq Cutoff |
| C10 | 470nF | Input DC decoupling Bass | Lower low freq Cutoff | Higher low freq Cutoff |
| C11 | Not mounted | See notes | | |
| C6,C7,C12 | 100nF | DC Vol. bypass | | |
| C5,C9 | 1000uF | Output Dc decoupling | Lower low freq Cutoff | Higher low freq Cutoff |
| C13 | 1uF | | | |
| C14 | 47uF | SVR | Increase of SVR , increase of switch ON time | Degradation of SVR |

## 4.2 Evaluation Board Functional Description:

### 4.2.1 Input Cut-off frequency:

The input Cut-off frequency is set by the external capacitor (C4,C8,C10) values and by the internal Input Impedance Rin ( 30KΩ typ)

fi (cut-off) = 1 / 2π ( Ri x Ci)

for the suggested values we have

Left/Right f i = 1 / 2π (30KΩ x 220nF) = 24Hz

SW fi = 1 / 2π (30KΩ x 470nF) = 11Hz

### 4.2.2 Output Cut-off frequency:

The output Cut-off frequency is set by the DC decoupling capacitor placed in series to the speaker (C5,C9) value and by the Speaker Impedance

| C5,C9 | 8ohm | 6ohm | 4ohm | Unit |
|---|---|---|---|---|
| 100uF | 199 | 265 | 398 | Hz |
| 220uF | 90 | 121 | 181 | Hz |
| 470uF | 42 | 56 | 85 | Hz |
| 1000uF | 20 | 27 | 40 | Hz |
| 2200uF | 9 | 12 | 18 | Hz |

### 4.2.3 Crossover Network for SW:

with this board it's possible, when the Bass Audio Signal to be sent to CH.3 is not available from the Audioprocessor, to generate it with a simple Low Pass Filter composed by an RC network.

The components to be added are R3,R6,C11:

$$fo = 1 / 2\pi \; R3 \; (R4) \; x \; C11$$

example:

for R3 = R4 = 4K7

we have C11 = 100nF → 340Hz

C11 = 220nF → 150Hz

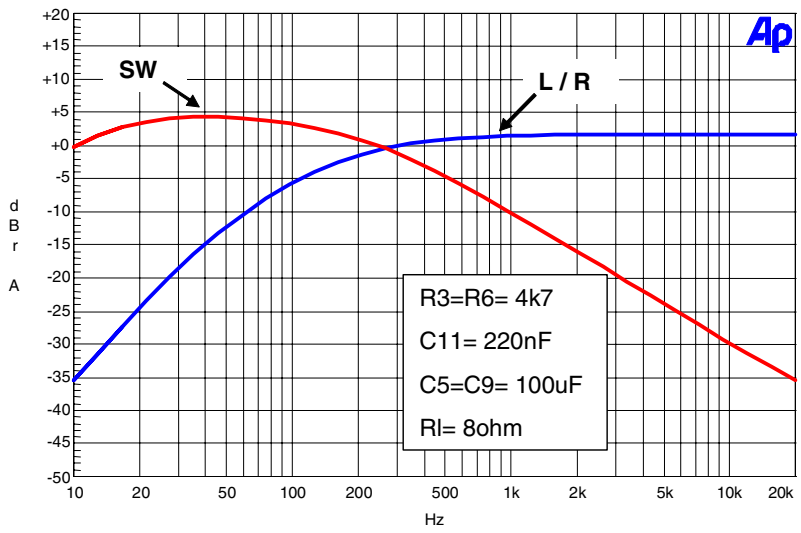
C11 = 330nF → 100Hz

It is advisable at this point to modify the value of the DC decoupling capacitors in such a way to send to L and R speakers only the high frequencies.

For example the frequency response shown in *Figure 8.* was obtained with Rl = 8ohm, C5=C9= 100uF, R3=R6= 4K7 and C11=220nF

Note: In order to give the input freq response less sensitive to the spread in the Input Impedance (Rin parameter) , it is possible to add externally two resitors R2,R7 in parallel to Rin.

**Figure 8. Frequency response**



# 5 General structure

## 5.1 Gain Internally Fixed to 20dB in Single Ended, 26dB in Bridge

Advantages of this design choice are in terms of:

- components and space saving
- output noise, supply voltage rejection and distortion optimization.

## 5.2 Silent Turn On/Off and Muting/Stand-by Function

The stand-by can be easily activated by means of a CMOS level applied to pin 9 through a RC filter.

Under stand-by condition the device is turned off completely (supply current = 1mA typ.; output attenuation= 80dB min.).

Every ON/OFF operation is virtually pop free. Furthemore, at turn-on the device stays in muting condition for a time determined by the value assigned to the SVR capacitor. While in muting the device outputs becomes insensitive to any kinds of signal that may be present at the input terminals. In other words every transient coming from previous stages produces no unplesantacoustic effect to the speakers.

## 5.3 STAND-BY DRIVING (pin9)

Some precautions have to be taken in the definition of stand-by driving networks: pin 9 cannot be directly driven by a voltage source whose curent capability is higher than 5mA. In pratical cases a series resistance has always to be inserted, having it the double purpose of limiting the current at pin 9 and to smooth down the stand-by ON/OFF transitions - in combination with a capacitor - for output pop prevention.

In any case, a capacitor of at lest 100nF from pin 9 to S-GND, with no resistance in between, is necessary to ensure correct turn-on.

## 5.4 Output Stage

The fully complementary output stage was made possible by the development of a new component: the ST exclusive power ICV PNP.

A novel design based upon the connection shown in *Figure 9.* has then allowed the full exploitation of its possibilities.

The clear advantages this new approach has over classical output stages are as follows:

## 5.5 Rail-to-Rail Output Voltage Swing With No Need of Bootstrap Capacitors.

The output swing is limited only by the $V_{CEsat}$ of the output transistors, which are in the range of 0.3Ω ($R_{sat}$) each.

Classical solutions adopting composite PNP-NPN for the upper output stage have higher saturation loss on the top side of the waveform.

This unbalanced saturation causes a significant power reduction. The only way to recover power consists of the addition of expensive bootstrap capacitors.

## 5.6 Absolute Stability Without Any External Compensation.

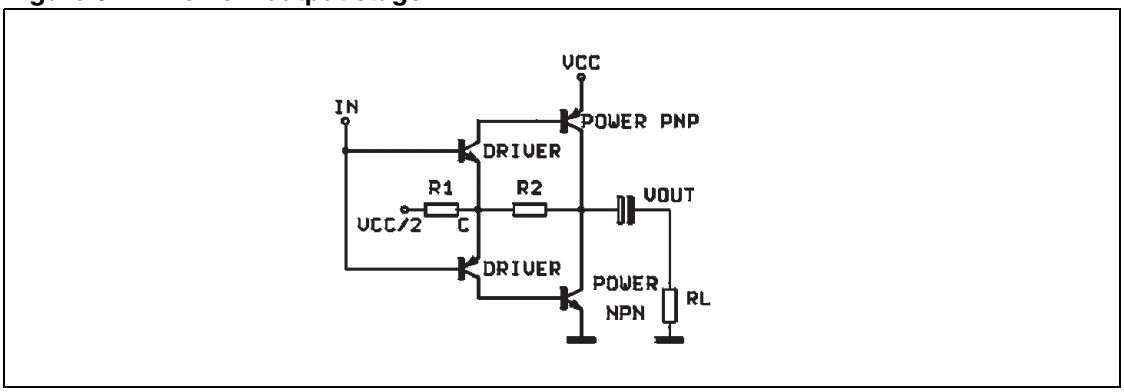
Referring to the circuit of *Figure 9.* the gain $V_{out}/V_{in}$ is greater than unity, approximately 1+R2/R1. The DC output (VCC/2) is fixed by an auxiliary amplifier common to all the channels.

By controlling the amount of this local feedback it is possible to force the loop gain (A*β) to less than unity at frequency for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

Most remarkably, the above feature has been achieved in spite of the very low closed loop gain of the amplifier.

In contrast, with the classical PNP-NPN stage, the solution adopted for reducing the gain at high frequencies makes use of external RC networks, namely the Boucherot cells.

**Figure 9. The new output stage**




## 5.7 BUILT–IN Shortcircuit Protection

Reliable and safe operation, in presence of all kinds of short circuit involving the outputs is assured by BUILT-IN protectors. Additionally to the AC/DC short circuit to GND, to VS, across the speaker, a SOFT SHORT condition is signalled out during the TURN-ON PHASE so assuring correct operation for the device it self and for the loudspeaker.

This particular kind of protection acts in such a way to avoid the device is turned on (by ST-BY) when a resistive path (less than 16 ohms) is present between the output and GND. As the involved circuitry is normally disabled when a current higher than 5mA is flowing into the ST-BY pin, it is important, in order not to disable it, to have the external current source driving the STBY pin limited to 5mA.

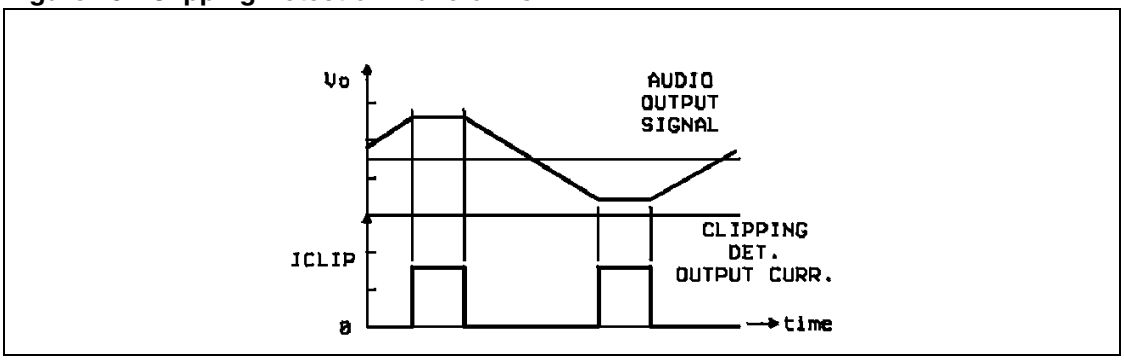
### 5.7.1 Diagnostic Facilities (Pin 12)

The STA543SA is equipped with a diagnostic circuitry able to detect the following events:

- Clipping in the output signal
- Thermal shutdown
- Output fault:
  - short to GND
  - short to VS
  - soft short at turn on

The information is available across an open collector output (pin 12) through a current sinking when the event is detected

**Figure 10. Clipping Detection Waveforms**




A current sinking at pin 12 is provided when a certain distortion level is reached at each output. This function allows gain compression facility whenever the amplifier is overdriven.

### 5.7.2 Thermal Shutdown

In this case the output 12 will signal the proximity of the junction temperature to the shutdown threshold. Typically current sinking at pin 12 will start ~10°C before the shutdown threshold is reached.

**Figure 11. Output fault waveforms**

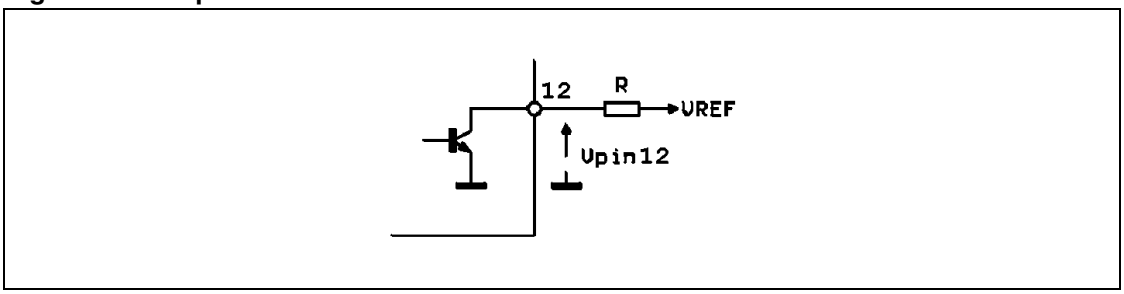
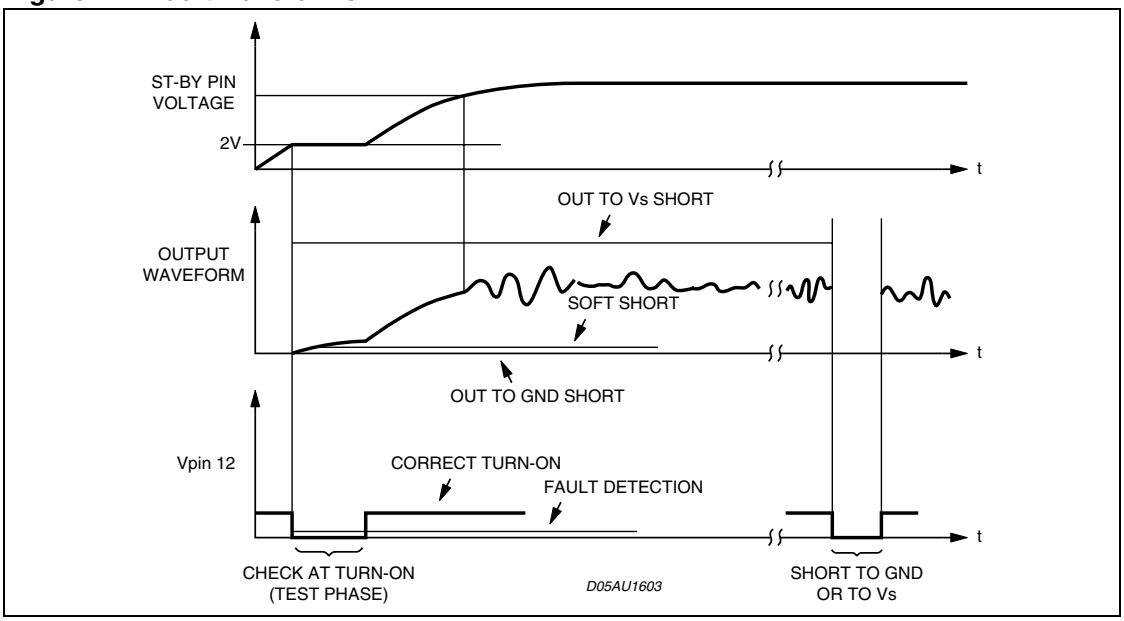


**Figure 12. Fault waveforms**




## 5.8 Handling of the diagnostic information

As different kinds of information is available at the same pin (clipping detection, output fault, thermal proximity), this signal must be handled properly in order to discriminate the event.

This could be done taking into account the different timing of the diagnostic output during each case.

Normally the clip detector signalling produces a

low level at out 12 that present under faulty conditions: based on this assumption an interface circuitry to differentiate the information is the represented in the schematic of *Figure 14.*

**Figure 13. Waveforms**

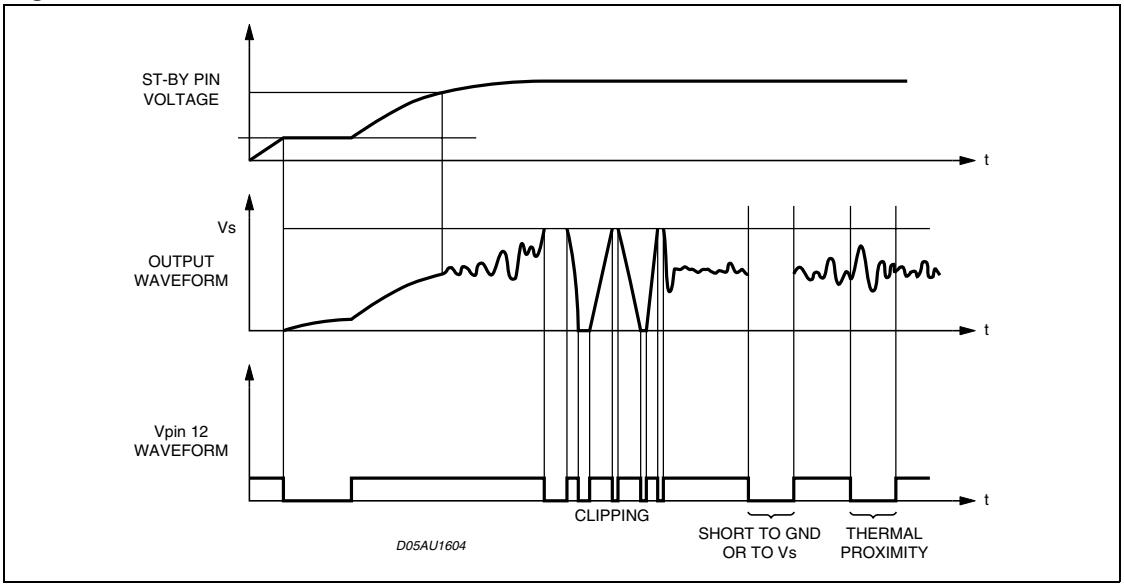
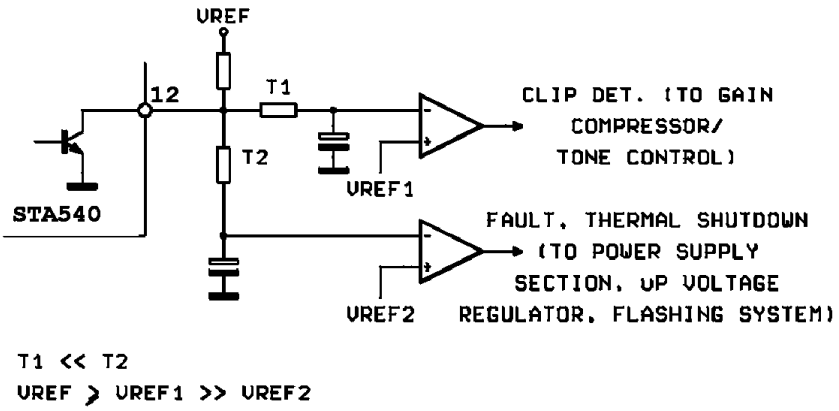


**Figure 14.**




## 5.9 PCB-Layout Grounding (general rules)

The device has 2 distinct ground leads, P-GND (POWER GROUND) and S-GND (SIGNAL GROUND) which are practically disconnected from each other at chip level. Proper operation requires that P-GND and S-GND leads be connected together on the PCB-layout by means of reasonably low-resistance tracks.

As for the PCB-ground configuration, a star-like arrangement whose center is represented by the supply-filtering electrolytic capacitor ground is highly advisable. In such context, at least 2 separate paths have to be provided, one for P-GND and one for S-GND.

The correct ground assignments are as follows:

- STANDBY CAPACITOR, pin 9 (or any other standby driving networks): on S-GND
- SVR CAPACITOR (pin 8): on S-GND and to be placed as close as possible to the device.
- INPUT SIGNAL GROUND (from active/passive signal processor stages): on S-GND.
- SUPPLY FILTERING CAPACITORS (pins 3,17): on P-GND. The (-) terminal of the electrolytic capacitor has to be directly tied to the battery (-) line and this should represent the starting point for all the ground paths.

# 6 Thermal Information

In order to avoid the thermal protection intervention that is placed at $T_j$=150°C (Thermal Muting) or $T_j$=160°C (Thermal Shut-down), it is important the Heat Sinker $R_{TH}$ (°C/W) dimensioning.

The parameters that influence the dimensioning are:

- Maximum dissipated power for the device ($P_{d\,max}$)
- Max.Thermal resistance Junction to case ($R_{THj\text{-}c}$)
- Max. Ambient temperature Tamb. Max

There is also an additional term that depends on the Iq (quiescent current).

## 6.1 Example (A): 2 channels Single Ended + 1Ch (BTL)

$V_{CC}$= 14.4V, $R_{load}$ = 2x 4Ω (SE) + 1x 4Ω (BTL)

Pout = 2 x 7W + 1 x 24W

$$P_{dmax} = 2 \cdot \frac{Vcc^2}{2\pi^2 R1} + \frac{2Vcc^2}{\pi^2 R1} = 2 \cdot 2.62 + 10.5 = 15.76W$$

$$\text{(Heat sink) } R_{THc\text{-}a} = \frac{150 - T_{ambmax}}{P_{dmax}} - R_{THj-c} = \frac{150 - 50}{15.76} - 2 = 4.3\ °C/W$$

NOTE: The values found gives an heatsinker that is dimensioned to sustain the max. dissipated power, but as explained in the Application Note (AN1965) the heatsinker can be smaller when we consider the real application where a musical program is used.

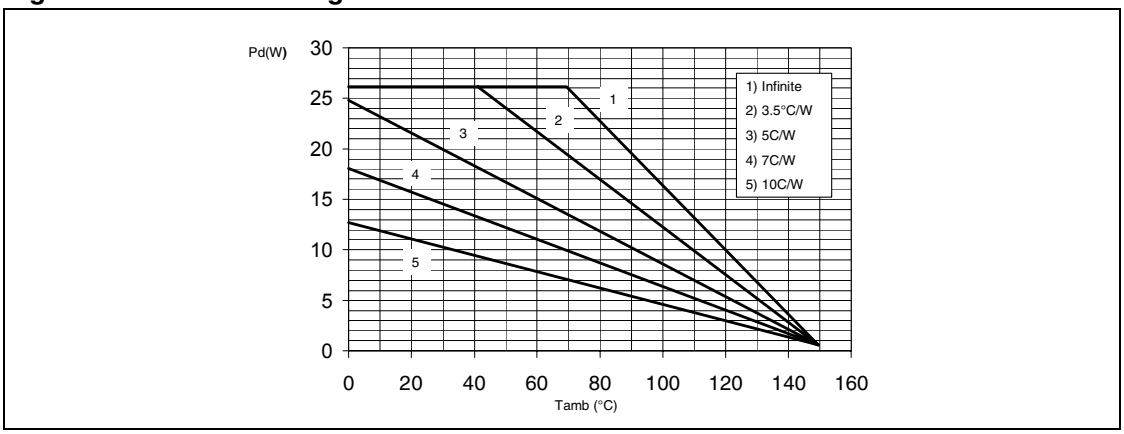
If we consider the so called "Average Listening Dissipated Power" concept we obtain a value that is about 40% less respect the Pdmax (see AN1965 for reference).

So in the examples (A) and we will obtain the value for the Average Listening Dissipated Power that is respectively:

-Example (A) : 15.76 W - 40% = 9.45W that gives $R_{THc\text{-}a}$ = 8.5°C/W

In *Figure 15.* is shown the Power Derating curve for the device

**Figure 15. Power Derating Curve**

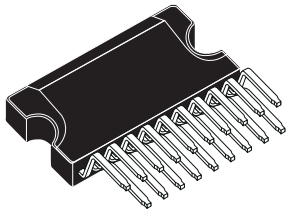


# 7 Package information

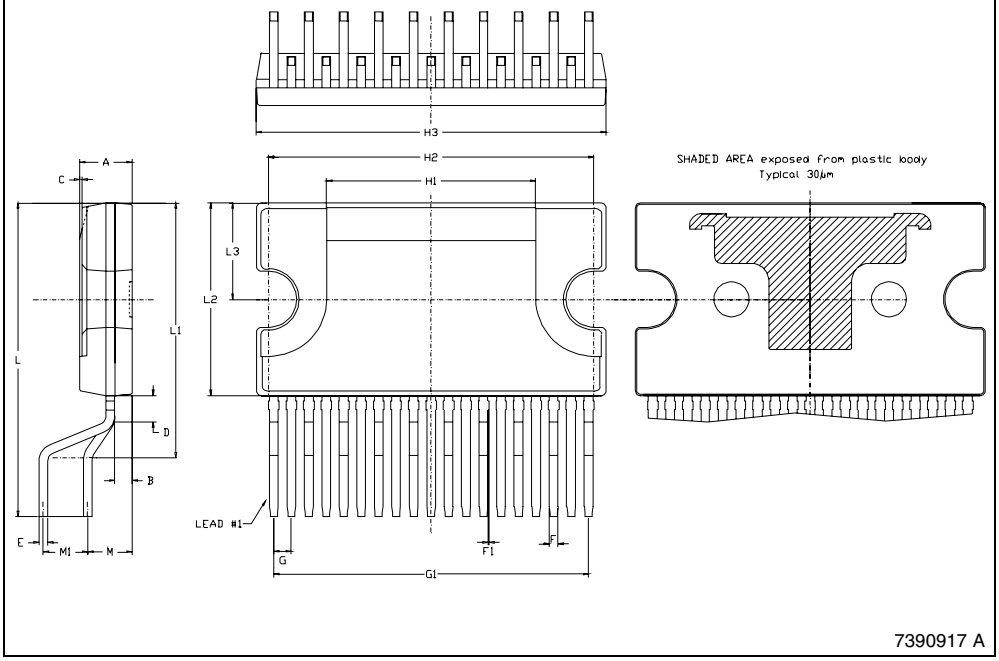
**Figure 16. Clipwatt 19 Mechanical Data & Package Dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 3.2 | | | 0.126 |
| B | | | 1.05 | | | 0.041 |
| C | | 0.15 | | | 0.006 | |
| D | | 1.50 | | | 0.061 | |
| E | 0.49 | | 0.55 | 0.019 | | 0.022 |
| F | 0.47 | 0.50 | 0.58 | 0.018 | | 0.020 |
| F1 | | | 0.1 | | | 0.004 |
| G | 0.87 | 1.00 | 1.13 | 0.034 | 0.039 | 0.044 |
| G1 | 17.87 | 18.0 | 18.13 | 0.703 | 0.708 | 0.713 |
| H1 | | 12.0 | | | 0.480 | |
| H2 | | 18.6 | | | 0.732 | |
| H3 | 19.85 | | | 0.781 | | |
| L | | 17.9 | | | 0.704 | |
| L1 | | 14.55 | | | 0.572 | |
| L2 | 10.7 | 11.0 | 11.2 | 0.421 | 0.433 | 0.441 |
| L3 | | 5.50 | | | 0.217 | |
| M | | 2.54 | | | 0.100 | |
| M1 | | 2.54 | | | 0.100 | |

**OUTLINE AND MECHANICAL DATA**



**Clipwatt19**



# 8 Revision history

| Date | Revision | Changes |
|---|---|---|
| 12-July-2005 | 1 | Initial release. |
| 28-July-2005 | 2 | Modified figgs 6 and 7. |

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